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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/663,832	ANATI ET AL.
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,16 and 18-51* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,16 and 18-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

1.   Claims 1-12, 16, and 18-51 have been examined.

Acknowledgment of papers filed: amendments and remarks filed on 26 October

2006. The papers filed have been placed on record.

Non-compliance

2.   Examiner reminds Applicant to assure that the claim amendments are in

compliance with the requirements set in the MPEP. Various limitations that were added

as an amendment were not underlined as required. For example, in claim 1, "stored in

a programmable logic array" was not underlined.

Specification

The title is not descriptive. A new title is required that is clearly indicative of the

invention to which the claims are directed.

The following title is suggested: Processor and Method for Micro-operations

Generation Using Fused Instructions.

Claim Objections

3.   Objection has been withdrawn.

Claim Rejections - 35 USC § 101

4.   35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
conditions and requirements of this title.

Additionally, 35 U.S.C. 101 requires the following:

The claimed invention as a whole must be useful and accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373-74, 47 USPQ2d at 1601-02. The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a Sec. 101 judicial exception, in that the process claim must set forth a practical application of that Sec. 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[A]n application of a law of nature or mathematical formula to a . . . process may well be deserving of patent protection." Diehr, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

5.   Claims 22-51 are rejected under 35 U.S.C. 101 because they lack a tangible result.

Regarding claims 49-50, "decoding" is not considered to be a tangible result.

Regarding the remaining claims, Applicant's claim language regarding "generating an indication" and "selecting values" do not appear to have a tangible result because they only claim a technique of choosing a value, rather than a final, tangible result of, for example, storing the chosen values.

Examiner asserts that the language of claims 22-51 although directed toward an apparatus, have limitations that disclose the intended use of these physical elements, rather than being limited to a mere composition of parts. Consequently, although Examiner agrees with Applicant's contention that "these elements are tangible elements", these claims do not contain a tangible result.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or
in public use or on sale in this country, more than one year prior to the date of application for
patent in the United States.

7.   Claims 7-12 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated

by Col (U.S. Patent No. 6,330,657).

8.   Regarding claim 7, Col discloses a method comprising:

decoding an instruction into a fused micro-operation (col 3 lines 46-56), including

selecting values of a field of said fused micro-operation based solely upon an indication

that said instruction is not being decoded into a simple micro-operation (col 3 lines 18-

21).

Note that a combined (fused) and an uncombined (simple) are the only two

instruction possibilities. Since these are mutually exclusive, then the decision of a

combined instruction is considered to be based "solely" on the indication that the

instruction is not simple.

Executing said fused micro-operation (fig. 4 references 412, 414, 416 and 418).

9.   Regarding claim 8, Col discloses the method of claim 7, further comprising:

generating said indication for said instruction from one or more fields of a micro-

operation template (col 3 lines 18-21).

Note that the "conflicting instructions" as described in the citation are determined based on dependencies in the opcodes--the opcodes being a particular field of a micro-operation template.

10.   Regarding claim 9, Col discloses the method of claim 7, wherein selecting values of said field includes selecting values of an operand of said fused micro-operation (col 8 lines 42-44).

11.   Regarding claim 10, Col discloses a method comprising:

Receiving an instruction to be decoded into a fused micro-instruction (col 5 lines 30-33 and col 3 lines 46-56),

decoding said (fig. 4 references 412, 414, 416 and 418) including selecting values of a first field of said fused micro-operation based solely upon an indication that said instruction is not being decoded into a simple micro-operation (col 3 lines 18-21) and a value decoded from a field of a micro-operation template that is used to select values of a second field of said fused micro-operation (Fig 6).

Note that, when the limitations of claims 11 and 12 are considered, this claim appears to be saying that the operand fields are selected to be put in a template based "solely" on the fact that an instruction is not a simple instruction and a "value" of the template used to selected an opcode of the combined instruction. Examiner considers that the "value" for selecting an opcode is the opcode itself. In particular, memory and

logical operations are often combined because they use different hardware and are

easily combinable without conflict. See fig. 6.

12.   Regarding claim 11, Col discloses the method of claim 10, wherein said first field

is an operand of said fused micro-operation (col 8 lines 42-44).

13.   Regarding claim 12, Col discloses the method of claim 10, wherein said second

field is an op-code of said fused micro-operation (col 17 lines 59-65).

14.   Regarding claim 19, Col discloses a method comprising:

Receiving an instruction to be decoded into a simple or fused micro-operation

((col 5 lines 30-300);

selecting values of a field of a micro-operation from a first set of physical traces

Note that paragraph 18 of Applicant's disclosure applears to describe a phyiscal

trace simply as registers to hold micro-operations.

If said micro-operation is simple and from a second set of physical traces if said

micro-operation is fused (col 3 lines 46-56),

Note that, clearly, two registers are only required for a combined instruction.

Where said micro-operation is generated from a micro-operation template that is

addressed by one or more instructions to be decoded into one or more fused micro-

operations (col 3 lines 46-56 and col 14 lines 36-44) and by one or more instructions to

be decoded into one or more simple micro-operations (fig 8).

15.   Regarding claim 20, Col discloses the method of claim 19, wherein selecting said

values comprises selecting said values based at least upon an indication whether said

instruction is being decoded into a fused micro-operation or into a simple micro-

operation (col 3 lines 46-56 and fig 8).

16.   Regarding claim 21, Col discloses the method of claim 19, wherein said field is

an operand of said micro-operation (fig 8 reference 708).

Claim Rejections - 35 USC § 103

17.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

18.   Claims 1-3, 16, 18, and 22-36 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Col in view of Moore (U.S. Patent No. 4,354,228).

19.   Regarding claim 1, Col/Moore discloses a method comprising:

Receiving an instruction to be decoded into a micro-operation;

Decoding said instruction including (col 5 lines 30-33)

selecting values for a field of a micro-operation based at least upon bits of a field

of a micro-operation template, wherein the number of said bits is fewer than the number

of bits in said field of said micro-operation (col 3 lines 46-56); and

Note that Applicant's claimed invention discloses a "template" for instructions.

These templates, as claimed later, contain particular fields. After considering

Applicant's disclosure, it appears that these templates are no more than a formatting for

instructions to be saved and these fields are no more than the formatted positions for

portions of an instruction (namely, opcodes, operands, etc). Consequently, the prior art

used contains, in the citation provided, two registers to hold the combined instructions.

These registers clearly must contain formatting positions for the opcodes, operands and

all necessary "fields" of the instruction. So, the bit positions of these instruction parts

are considered to be fields and the formatting required for the disclosed instruction

registers are considered to be a template.

Executing said micro-instructions (fig. 4 references 412, 414, 416 and 418).

Col fails to disclose a programmable logic array to contain the hardware with the micro-

operation template.

Moore discloses designing a processor utilizing a PLA (col 5 lines 56-59).

Col would have been motivated to utilize a PLA design for its processor due to

flexibility. A PLA is reprogrammable, so it can be changed periodically to accommodate

different circumstances. One example in particular disclosed in Moore is the ability to

switch instruction sets (col 5 lines 56-69).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Col and allow it to be implemented in a programmable logic array as shown in Moore.

20.   Regarding claim 2, Col/Moore discloses the method of claim 1, wherein selecting said values includes selecting said values if said micro-operation is a fused micro-operation (col 3 lines 46-52).

21.   Regarding claim 3, Col/Moore discloses the method of claim 2, wherein selecting said values includes selecting said values for an op-code of said micro-operation (col 3 lines 46-56).

22.   Regarding claim 16, Col/Moore discloses a method comprising:

Receiving a first instruction to be decoded into one or more fused micro-operations (col 3 lines 46-56),

addressing a micro-operation template stored in a programmable logic array (Moore col 5 lines 56-59) by said first instruction (fig. 4 reference 406);

receiving a second instruction to be decoded into one or more simple micro-operations (col 14 lines 34-45);

addressing said micro-operation template by said second instruction (fig 4 reference 406);

for each of said first instruction and second instruction, generating an indication

whether the instruction is to be decoded into a fused micro-operation or into a simple

micro-operation (col 3 lines 18-21); and

executing said fused or simple micro-instruction (fig. 4 references 412, 414, 416,

and 418).

23.   Regarding claim 18, Col/Moore discloses the method of claim 17, wherein

generating said indication comprises generating said indication from one or more fields

of said micro-operation template and from bits extracted directly from said first or

second instruction (fig. 8 reference 708).

24.   Regarding claim 22, Col/Moore discloses a processor to execute instructions (col

1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference 404)

including at least:

A programmable logic array (Moore col 5 lines 56-59) to store a micro-operation

template to be addressed by an instruction during decoding of said instruction into a

fused micro-operation having a particular field (col 3 lines 46-56).

a micro-operation template to be addressed by an instruction during decoding of

said instruction into a fused micro-operation having a particular field (col 3 lines 46-56);

and a multiplexer to select values for said particular field based at least upon bits of a

field of said micro-operation template (col 3 lines 46-56),

Note that there are two micro-instruction registers. As cited, two are used during a combined instruction suggesting that this wouldn't be the case if the instructions are uncombinable. The American Heritage College Dictionary definition of a multiplexer is "a device that can interleave two or more activities". Clearly, in this case, the decision whether or not to route the second instruction to the second, parallel register is completed by a multiplexer.

Wherein the number of said bits is fewer than the number of bits in said particular field.

25.   Regarding claim 23, Col/Moore discloses the processor of claim 22, wherein said particular field is an op-code of said fused micro-operation (col 8 lines 42-44).

Note that this "particular field" is not very limited. The instruction is considered to have many "particular fields" including an opcode and operands.

26.   Regarding claim 24, Col/Moore discloses the processor of claim 22, wherein said multiplexer is to select values for said particular field also based upon an indication that said instruction is not being decoded into a simple micro-operation (col 3 lines 46-56).

27.   Regarding claim 25, Col/Moore discloses a processor to execute instructions, the processor comprising: an instruction decoder (fig 4 reference 404) including at least: a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a

particular field (Moore col 5 lines 56-59); and a multiplexer to select values for said

particular field based solely upon an indication that said instruction is not being decoded

into a simple micro-operation (col 3 lines 46-56).

28.   Regarding claim 26, Col/Moore discloses the processor of claim 25, wherein said

particular field is an operand of said fused micro-operation (col 8 lines 42-44).

29.   Regarding claim 27, Col/Moore discloses the processor of claim 25, wherein said

indication comprises bits of a field of said micro-operation template (fig 8).

   Note that the opcodes and operands determine whether or not an instruction can

be combined, necessary information considered to be comprised by the indication.

30.   Regarding claim 28, Col/Moore discloses the processor of claim 25, wherein said

instruction decoder further comprises: a decoder (fig 4 reference 404) to generate said

indication from two or more fields of said micro-operation template and from bits

extracted directly from said instruction (fig 8).

31.   Regarding claim 29, Col/Moore discloses a processor to execute instructions (col

1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference 404)

including at least: a programmable logic array to store a micro-operation template to be

addressed by an instruction during decoding of said instruction into a fused micro-

operation having a particular field (Moore col 5 lines 56-59); a decoder (fig 4 reference

404) to decode a value from a field of said micro-operation template (col 14 lines 35-
45); and a multiplexer to select values for said particular field based solely upon said
value and an indication that said instruction is not being decoded into a simple micro-
operation (col 3 lines 46-56).

32.   Regarding claim 30, Col/Moore discloses the processor of claim 29, wherein said
field of said micro-operation template is used to select values of an op-code of said
fused micro-operation (col 3 lines 46-56).

33.   Regarding claim 31, Col/Moore discloses the processor of claim 29, wherein said
particular field is an operand of said fused micro-operation (col 8 lines 42-44).

34.   Regarding claim 32, Col/Moore discloses the processor of claim 29, wherein said
indication comprises bits of another field of said micro-operation template (fig 8).

        Note that the indication comprises bits from the operand field and the opcode
field.

35.   Regarding claim 33, Col/Moore discloses the processor of claim 29, wherein said
instruction decoder further comprises: a decoder to generate said indication from two or
more additional fields of said micro-operation template and from bits extracted directly
from said instruction (fig 8).

Note that the "two or more fields" can include any operands or opcodes from the second instruction. These bits are considered to be extracted directly as well.

36.   Regarding claim 34, Col/Moore discloses a processor to execute instructions (col 1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference 404) including at least: a programmable logic array (Moore col 5 lines 56-59) to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations (col 3 lines 46-56).

37.   Regarding claim 35, Col/Moore discloses the processor of claim 34, wherein said micro-operation template includes a field having a value that identifies that both a fused micro-operation and a simple micro-operation can be generated from said micro-operation template (col 3 lines 46-56).

38.   Regarding claim 36, Col/Moore discloses the processor of claim 34, wherein said instruction decoder further comprises: a decoder to generate an indication for a particular instruction from two or more fields of said micro-operation template (fig 8) and from bits extracted directly from said particular instruction (fig 8),

Note that these fields "of said micro-operation template" and those "bits extracted directly" are considered to be in the same category of bits (operands and opcodes from the instruction).

Wherein said indication is an indication whether said particular instruction is to be decoded into a fused micro-operation or into a simple micro-operation (fig 8).

39.   Claims 37-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col/Moore (as previously combined) in further view of Takeda (U.S. Patent No. 6,643,720).

40.   Regarding claim 37, Col/Moore discloses an apparatus comprising: a processor to execute instructions (col 1 lines 26-27), the processor comprising: an instruction decoder including at least: a programmable logic array (Moore col 5 lines 56-59) to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field (col 3 lines 46-56); and a multiplexer to select values for said particular field based at least upon bits of a field of said micro-operation template (col 3 lines 46-56), wherein the number of said bits is fewer than the number of bits in said particular field (fig 8).

Note that the language of this claim is somewhat confusing. Initially, the claim states that values are selected based "at least" upon bits of a field. This appears to mean that if a field has 5 bits, "the bits" as described in the claim could be anywhere between 2 and 5 bits. Then, the claim later says that "said bits" are fewer than the number of bits in the particular field. So, based on the language used, "said bits" are considered to be any two bits of any field utilized in the determination made in fig. 8.

Col/Moore fails to disclose a voltage monitor.

Takeda discloses a voltage monitor (col 14 lines 45-48).

As shown in Takeda, the voltage monitor utilizes a watchdog timer, which is a

mechanism used to restart the main program due to a problem. This, of course,

prevents an improper voltage amount from having a negative impact on the system.

Col/Moore would be motivated to utilize a voltage monitor for this reason.

It would have been obvious at the time of the invention for one of ordinary skill in

the art to take the computing system of Col/Moore and utilize a voltage monitor as

shown in Takeda.

41.   Regarding claim 38, Col/Moore/Takeda discloses the apparatus of claim 37,

wherein said particular field is an op-code of said fused micro-operation (fig 8).

42.   Regarding claim 39, Col/Moore/Takeda discloses the apparatus of claim 37,

wherein said multiplexer is to select values for said particular field also based upon an

indication that said instruction is not being decoded into a simple micro-operation (col 3

lines 46-56).

43.   Regarding claim 40, Col/Moore/Takeda discloses an apparatus comprising: a

voltage monitor (Takeda col 14 lines 45-48); and a processor to execute instructions

(col 1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference

404) including at least: a programmable logic array (Moore col 5 lines 56-59) to store a

micro-operation template to be addressed by an instruction during decoding of said .

instruction into a fused micro-operation having a particular field (col 3 lines 46-56); and

a multiplexer to select values for said particular field based solely upon an indication

that said instruction is not being decoded into a simple micro-operation (col 3 lines 46-

56).

44.   Regarding claim 41, Col/Moore/Takeda discloses the apparatus of claim 40,

wherein said particular field is an operand of said fused micro-operation (fig. 8 reference

708).

45.   Regarding claim 42, Col/Moore/Takeda discloses the apparatus of claim 40,

wherein said indication comprises bits of a field of said micro-operation template (fig 7

reference 706 or 708).

46.   Regarding claim 43, Col/Moore/Takeda discloses the apparatus of claim 40,

wherein said instruction decoder further comprises: a decoder to generate said

indication from two or more fields of said micro-operation template and from bits

extracted directly from said instruction (fig 7 reference 706 and 708).

47.   Regarding claim 44, Col/Moore/Takeda discloses an apparatus comprising: a

voltage monitor (Takeda col 14 lines 45-48); and a processor to execute instructions

(col 1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference

404) including at least: a programmable logic array (Moore col 5 lines 56-59) to store a

micro-operation template to be addressed by an instruction during decoding of said

instruction into a fused micro-operation having a particular field (col 3 lines 46-56); a

decoder to decode a value from a field of said micro-operation template (col 14 lines 35-

45); and a multiplexer to select values for said particular field based solely upon said

value and an indication that said instruction is not being decoded into a simple micro-

operation (col 3 lines 46-56).

48.   Regarding claim 45, Col/Moore/Takeda discloses the apparatus of claim 44, ·

wherein said field of said micro-operation template is used to select values of an op-

code of said fused micro-operation (col 3 lines 46-56).

   Note that the since a fused instruction executes in paralell, then the timing of the

op-code selection is affected, meaning that "said field" us used to select a value of the

opcode.

49.   Regarding claim 46, Col/Moore/Takeda discloses the apparatus of claim 44,

wherein said particular field is an operand of said fused micro-operation (col 8 lines 42-

44).

50.   Regarding claim 47, Col/Moore/Takeda discloses the apparatus of claim 44,

wherein said indication comprises bits of another field of said micro-operation template

(fig 8).

51.. Regarding claim 48, Col/Moore/Takeda discloses the apparatus of claim 44, wherein said instruction decoder further comprises: a decoder to generate said indication from two or more additional fields of said micro-operation template and from bits extracted directly from said instruction (fig 8).

52. Regarding claim 49, Col/Moore/Takeda discloses an apparatus comprising: a voltage monitor (Takeda col 14 lines 45-48); and a processor to execute instructions (col 1 lines 26-27), the processor comprising: an instruction decoder (fig 4 reference 404) including at least: a programmable logic array (Moore col 5 lines 56-59) to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations (col 3 lines 46-56).

53. Regarding claim 50, Col/Moore/Takeda discloses the apparatus of claim 49, wherein said micro-operation template includes a field having a value that identifies that both a fused micro-operation and a simple micro-operation can be generated from said micro-operation template (col 3 lines 46-56).

Note that this is considered to be true since both the fused and simple instructions contain opcodes and operands, fields that are the same whether or not the instruction is combined or not.

54.   Regarding claim 51, Col/Moore/Takeda discloses the apparatus of claim 49,

wherein said instruction decoder further comprises: a decoder to generate an indication

for a particular instruction from two or more fields of said micro-operation template and

from bits extracted directly from said particular instruction, wherein said indication is an

indication whether said particular instruction is to be decoded into a fused micro-

operation or into a simple micro-operation (col 3 lines 46-56).

Response to Arguments

55.   Applicant's arguments filed 20 November 2006 have been fully considered but

they are not persuasive.

56.   Applicant states:

"Independent claim 1 recites 'selecting values for a field of said micro-operation

based at least upon bits of a field of a micro-operation template stored in a

programmable logic array, wherein the number of said bits is fewer than the number of

bits in said field of said micro-operation."

After a careful review of the language in this claim, it appears to not be very

limiting. The phrases "at least upon" and "wherein the number of bits is fewer" appear

to cancel each other out.

For example, claim 1 discloses, "selecting values for a field of said micro-

operation based at least upon bits of a field of micro-operation template." Let's say, for

instance, that there is a field that contains 5 bits and all of them are required for

"selecting values for a field of said micro-operation." Examiner can choose 3 of those

bits, which are considered to be "bits of a field of a micro-operation template". In this

circumstance, it is true that the selecting is based "at least upon" these bits. It is also

true that "the number of bits is fewer than the number of bits in said field"

All limitations of this claim are satisfied.

57.   Applicant states:

"Independent claim 7 recites 'decoding an instruction into a fused micro-

operation' and further 'selecting values of a field of said fused micro-operation based

solely upon an indication that said instruction is not being decoded into a simple

instruction."

An uncombined (simple) instruction has various registers associated with the

instruction—let's say two. A combined (fused) instruction will have those registers as

well as other registers associated with the second instruction—let's say another two.

Now, if the instruction is fused, then all four register values will be selected. If the

instruction is not fused, then only the first two registers will be selected. This is

considered to be "selecting values of a field of said fused micro-operation based solely

upon an indication that said instruction is not being decoded into a simple instruction"

It appears from the disclosure on pages 9 and 10, Applicant's invention uses the

same rational for the language in the claims.

58.   Applicant states:

"Independent claim 10 recites 'receiving an instruction to be decoded into a fused

micro-operation' and further 'selecting values of a first field of said fused micro-

operation based solely both upon an indication that said instruction is not being

decoded into a simple micro-operation and upon a value decoded from a field of said

micro-operation template is used to select values of a second field of said fused micro-

operation."

The "value" claimed sounds like the opcode of an instruction. It is a decoded·

value that is used to select a second field (operands) of a fused micro-operation. The

opcode (or type of instruction) is used as part of the determination as to whether an

instruction should be combined (fused). So, it is also a factor in selecting values.

Examiner asserts that the arguments above address the concerns of the

remaining independent claims.

Conclusion

59.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

· A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

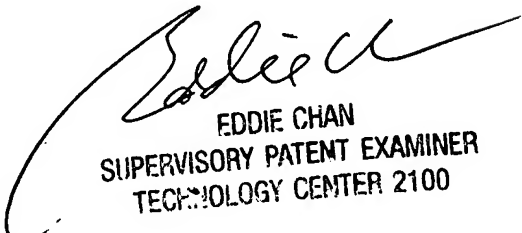TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100